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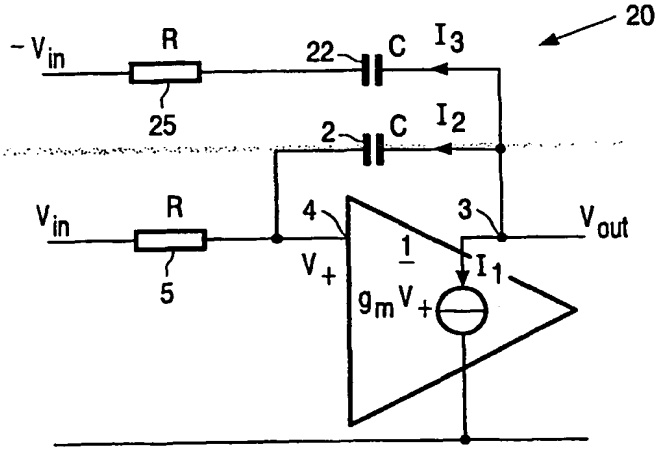
(54) Title: OPERATIONAL AMPLIFIER INTEGRATOR



(57) Abstract: An integrator circuit comprises an operational amplifier which has a transistor stage (1) with an input terminal (4) and an output terminal (3), a feedback capacitor (2) connected between the input terminal (4) and the output terminal (3), and a resistor (5) connected to the input terminal (4), and also has an additional circuit branch (20) comprising a second capacitor (22) and a second resistor (25) connected in series one with the other and connected between the output terminal (3) of the transistor stage (1) and voltage comprising the inverted input voltage to the integrator circuit. Preferably two additional circuit branches (320, 320') are provided. One may be connected between the non-inverting or positive output terminal (33) of the transistor stage (1) and the inverting or negative input of the integrator. The other circuit may be connected between the negative output terminal (37) of the transistor stage (1) and the positive input of the integrator. This is particularly useful for balanced amplifier topology. The invention finds particular application in the first filter stage (integrator) in a sigma delta analog to digital conversion circuits and provide an improved operational amplifier integrator and particularly helps in compensating for a right halfplane zero.

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OPERATIONAL AMPLIFIER INTEGRATOR

The present invention relates to an operational amplifier (op amp) integrator.

It is known to construct integrator circuits from op amps by connecting a resistor to the input of a transistor circuit and using a capacitor as a feedback element. The ideal integrator has infinite gain and only a single pole when the frequency of the applied signal is zero. However, practical integrator circuits based on a transconductance stage have a zero in the right halfplane when the frequency of the applied signal is equal to the feedback capacitance divided by the transconductance of the transistor.

It is an object of the present invention to provide an improved operational amplifier integrator and particularly to compensate for the right halfplane zero.

According to the present invention there is provided

an integrator circuit comprising:

- a transistor stage
- a feedback capacitor connected between the input and the output of the transistor stage;
- a resistor connected to the input of the transistor stage;
- characterised by an additional circuit branch comprising:
- a second capacitor and a second resistor connected in series one with the other and connected between the output of the transistor stage and the inverted input to the integrator circuit.

Preferably two additional circuit branches are provided: one may be connected between the positive input and output of the transistor stage and one connected between the negative input and output. This is particularly useful for balanced amplifier topology. The transistor is an invertor and thus positive input voltages provide negative output voltages and vice versa.

The invention finds particular application in the first filter stage (integrator) in a sigma delta analog to digital conversion circuit. This first filter stage is very hard to design.

For a better understanding of the present invention and to show how the same may be carried into effect, reference will now be made to the accompanying drawings, in which:

Figure 1 is a circuit diagram of a conventional op amp integrator;

Figure 2 is a circuit diagram of one embodiment of an op amp integrator according to the present invention;

Figure 3 is a circuit diagram of a second embodiment of an op amp integrator according to the present invention using balanced amplifier topology;

Figure 4 is a circuit diagram of a third embodiment of an op amp integrator according to the present invention applied to a sigma delta analog to digital convertor circuit;

Figure 5 is a series of equations which apply to the known circuit of figure 1;

Figure 6 is a series of equations which apply to the circuit of the invention as shown in figure 2.

In figure 1 a prior art op amp integrator circuit (transconductance stage) is shown comprising, as is well known to a person skilled in the art, a transistor stage 1 having a transconductance g_m and an internal voltage V_+. A feedback capacitor 2 of value C is connected between a inverting output terminal 3 of the transistor and its non-inverting input terminal 4. A resistor 5 of value R is also connected to the non-inverting input terminal 4 to buffer the input voltage V_{in}. The inverting input terminal 6 is connected to ground. The voltage at the non-inverting output 3 of the transistor stage 1 is V_{out}.

The current to the feedback capacitor 2 is I_2 and this is given by the voltage across the capacitor 2 divided by the total impedence presented by the capacitor 2 and the resistor 5, and is given by equation 1 in figure 5. The current flowing through the transistor 1 to ground is I_1 as indicated and this is given by the voltage V_+ through the transistor stage 1 multiplied by its transconductance g_m, as shown by equation 2 in figure 5. The internal voltage V_+ of transistor stage 1 is given by equation 3.

Since the total current must be preserved in the circuit then the sum of the currents I_2 and I_1 must be zero, as indicated in equation 4. Thus, substituting equations 1 and 2 in equation 4 results in equation 5. The terms are rearranged in equation 6 showing that there is a zero in the right half plane. This is undesirable.

This zero can be compensated by the extra circuit branch which will be evident from a comparison of the known circuit of figure 1 with the new circuit of figure 2.

The extra circuit branch 20 has a current I_3 and comprises a second capacitor 22 and a second resistor 25 connected in series between an inverted input voltage $-V_{in}$ and the non-inverting output node 3 of the transistor stage 1.

The equations 7 to 13 in figure 6 illustrate how the extra circuit branch 20 compensates for the zero in the right half plane.

Equation 7 is the same as Equation 1 in figure 5 and gives the value of the current I_2 in the feedback branch comprising capacitor 2. Equation 8 gives the current I_3 in the xtra circuit branch 20, and equation 9 sums these two currents.

In equation 10 the formula for the internal voltage V_+ in the transistor stage 1 is set out and this leads to equation 11, giving the current I_1 through the transistor stage 1.

Equation 12 assumes that the current in the three branches must cancel out, ie that the three currents add up to zero, and equation 13 then effectively sums the currents I_1, I_2 and I_3 given by equations 11, 7 and 8 respectively.

In equation 14 the terms are simplified to give an equation for the ratio of the output voltage to the input voltage. As can be seen from a comparison of equation 14 giving this ratio for the new circuit of figure 2, with the equation 6 giving the ratio for the known circuit of figure 1, the new circuit compensates for the zero in the right halfplane, and this compensation is not dependent on the characteristic of the amplifier.

Figure 3 illustrates an op amp integrator using balanced amplifier topology, which is well known to persons skilled in the art. The bias amplifier is a transconductance so that a positive input voltage leads to a current sink at the output and hence a negative voltage at the output. The circuit is essentially the same as that in figure 2 but the circuit elements are repeated on the other side of the transistor stage 31 essentially in mirror image. Thus a first input voltage V_{in} is connected via a first input resistor 35a to a first input terminal 34 of transistor stage 31. A first feedback capacitor 32a is connected between the first input terminal 34 and a first output terminal 33 at which a first output voltage V_{out} appears.

An negative input voltage $-V_{in}$ is connected via a second input resistor 35b to a second input terminal 36 of transistor stage 31. A second feedback capacitor 32b is connected between the second input terminal 36 and the second output terminal 37 at which a negative output voltage $-V_{out}$ appears.

Two extra circuit branches, each comprising a capacitor and a resistor in series, are provided. A first extra circuit branch 320a comprises a capacitor 322a and a resistor 325a. This connects the negative input voltage $-V_{in}$ to the first output terminal 33 at which the positive output voltage V_{out} appears. A second extra circuit branch 320b comprises

a capacitor 322b and a resistor 325b. This connects the positive input voltage V_{in} to the output terminal 37 at which the negative output voltage $-V_{out}$ appears.

In figure 4 a circuit diagram is presented wherein the invention is applied to the first stage of a sigma delta analog to digital convertor. This circuit comprises the circuit elements shown in figure 3 and denoted by the same reference symbols and some additional resistors and output voltage lines. The additional resistors have a different value R2 to the resistors R1 shown in the previous figures. Each is connected between respective resistors R1 and capacitors C and an additional output voltage line. Thus resistor 41 connects resistor 325a to analog output voltage line 45 on which the positive analog voltage V_{DAC} appears. Resistor 42 connects input terminal 34 of transistor stage 31 to output line 45 (V_{DAC}).

Likewise resistor 43 connects resistor 325b to analog output voltage line 46 on which a negative analog voltage $-V_{DAC}$ appears. Resistor 44 connects input terminal 36 of transistor stage 31 to the inverting analog output line 46 ($-V_{DAC}$).

CLAIMS:

1. An integrator circuit comprising:
- an operational amplifier having:
- a transistor stage having an input terminal and an output terminal;
- a feedback capacitor connected between the input terminal and the output terminal of the transistor stage;
- a resistor connected to the input terminal of the transistor stage;
- characterised by
- an additional circuit branch comprising:
- a second capacitor and a second resistor connected in series one with the other and connected between the output terminal of the transistor stage and voltage comprising the inverted input voltage to the integrator circuit.

2. An integrator circuit according to claim 1 wherein a second additional circuit branch is provided.

3. An integrator circuit according to claim 2 wherein the first additional circuit branch is connected between the non-inverted output of the transistor stage and the inverted input of the integrator and the second additional circuit branch is connected between the inverted output terminal of the transistor stage and the non-inverted input of the integrator.

4. An integrator circuit according to any one of the preceding claims when comprising the first filter stage in a sigma delta analog to digital conversion circuit.

5. A sigma delta analog to digital conversion circuit comprising an integrator circuit according to any one of the preceding claims.

6. A balanced amplifier comprising an integrator circuit according to any one of the preceding claims.

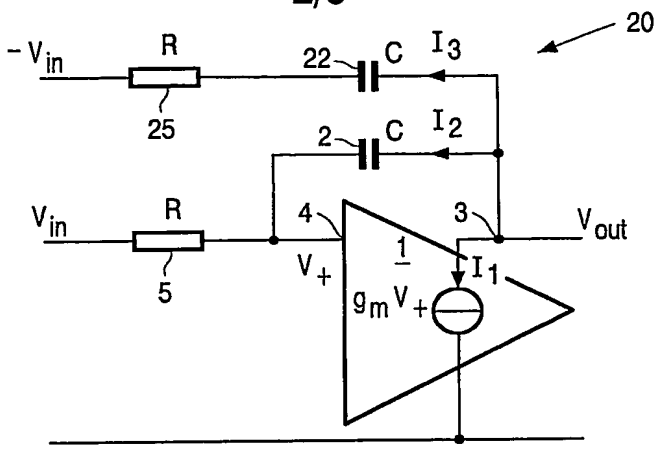

FIG. 2

$$I_2 = \frac{V_{out} - V_{in}}{1/sC + R} \qquad \text{Equation 7}$$

$$I_3 = \frac{V_{out} + V_{in}}{1/sC + R} \qquad \text{Equation 8}$$

$$I_2 + I_3 = \frac{2V_{out}}{1/sC + R} \qquad \text{Equation 9}$$

$$V_+ = \frac{V_{in}/sC + V_{out}\,R}{1/sC + R} \qquad \text{Equation 10}$$

$$\Rightarrow I_1 = \frac{g_m V_{in}/sC + g_m V_{out}\,R}{1/sC + R} \qquad \text{Equation 11}$$

$$I_1 + I_2 + I_3 = 0 \qquad \text{Equation 12}$$

$$g_m V_{in}/sC + g_m V_{out}\,R + 2V_{out} = 0 \qquad \text{Equation 13}$$

$$\frac{V_{out}}{V_{in}} = -\frac{1}{s(2/g_m + R)C} \qquad \text{Equation 14}$$

FIG. 6

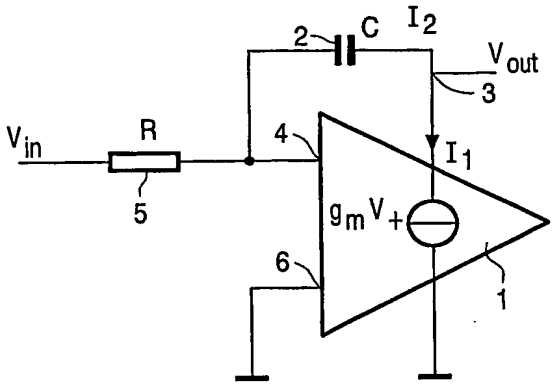

FIG. 1 PRIOR ART

$$I_2 = \frac{V_{out} - V_{in}}{1/sC + R} \qquad \text{Equation 1}$$

$$I_1 = g_m V_+ = \frac{g_m V_{in}/sC + g_m V_{out} R}{1/sC + R} \qquad \text{Equation 2}$$

$$V_+ = \frac{V_{in}/sC + V_{out} R}{1/sC + R} \qquad \text{Equation 3}$$

$$I_1 + I_2 = 0 \qquad \text{Equation 4}$$

$$\Rightarrow V_{out} - V_{in} + g_m V_{in}/sC + g_m V_{out} R = 0 \qquad \text{Equation 5}$$

$$\Rightarrow \frac{V_{out}}{V_{in}} = -\frac{1 - sC/g_m}{s(1/g_m + R)C} \qquad \text{Equation 6}$$

FIG. 5

INTERNATIONAL SEARCH REPORT

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A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 G06G7/186

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 G06G H03H

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, WPI Data, PAJ

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 4 633 223 A (SENDEROWICZ DANIEL) 30 December 1986 (1986-12-30) column 3, line 10 -column 4, line 61; figures 1,2	1-3

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Date of the actual completion of the international search	Date of mailing of the international search report
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Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31–70) 340–2040, Tx. 31 651 epo nl, Fax: (+31–70) 340–3016	Ledrut, P

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Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 4633223 A	30-12-1986	US 4574250 A	04-03-1986
		US 4633425 A	30-12-1986
		US 4599573 A	08-07-1986

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US 4633223 A	30-12-1986	US 4574250 A	04-03-1986
		US 4633425 A	30-12-1986
		US 4599573 A	08-07-1986

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European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31–70) 340–2040, Tx. 31 651 epo nl, Fax (+31–70) 340–3016	Ledrut, P

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